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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/628,083 | 07/24/2003 | Amit Ramchandran | 021202-003730US | 3515 |

37490 7590 07/12/2006

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| EXAMINER | |
|---|---|
| COLEMAN, ERIC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/628,083 | RAMCHANDRAN, AMIT | |
| | Examiner | Art Unit | |
| | Eric Coleman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-20* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fraser (patent No. 6,907,598) in view of Mohamed (patent No. 5,704,053).

3. Fraser taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Identifying frequently executed instruction in the set of instructions for an information processing device (e.g., see fig. 5); and

b) Replacing at least one instance of the frequently executed instruction with a compressed instruction referencing and index value (e.g., see fig. 5 and col. 3, lines 9-32 and col. 12-30).

4. Fraser further taught (claim 1,20) that the repeated instruction sequences were replaced with a compressed instruction (e.g., see col. 3, lines 9-32), but did not expressly detail inserting an explicit caching instruction in the set of instructions before the identified instruction, wherein the explicit caching instruction associates the identified instruction with at least one index value. . Mohamed however taught for repetitive instruction blocks such as loops placing long instruction words in an instruction buffer where a prefetch flag bit is generated that facilitates copying the

instructions from main memory to the prefetch instruction buffer. (e.g., see col. 2, lines 36-49). Mohamed taught that the prefetch instruction flag bit is sent from the compiler to the decoder. (e.g., see col. 3, lines 35-40) The Mohamed prefetch instruction flag bit is decoded several instructions before the prefetch instructions are decoded (e.g., see col. 3, lines 55-60). Since the use of the flag bit instructs the processor to perform an operation (namely prefetching of instruction(s) from main memory to cache) then it would have been obvious to one of ordinary skill the input to the decoder comprising the flag bit would have comprised an instruction. This is further evidenced since the decoder in the Mohamed system sends a signal to the prefetch instruction buffer control unit indicating the prefetch instruction flag bit was decoded and the prefetch instructions are to be written to a prefetch instruction buffer (e.g. col. 4 lines 1-7) and instructions are decoded from the compiler which are executed(e.g., see col. 3, lines 21-34). [Note the moving of instruction from main memory to a smaller faster buffer meet the claimed caching limitation and the mapping table is used by the instruction to associate the index with a instruction stored in a portion of memory e.g., see col. 4, lines 22-60 of Mohamed)].

5. It would have been obvious to one of ordinary skill to combine the teachings of Fraser and Mohamed. Both references were directed to the problems of processing repeated instructions in a DP system (e.g., see col. 2, lines 35-45 of Mohamed and col. 2, lines 10-31 of Fraser). The Fraser system is further directed to problems with embedded system such as handheld computer systems, telephones etc. that have a relatively small amount of space. And the solution set forth in Fraser is to compress the

instruction in the program replacing repetitive instruction with a Echo instruction ahead of time and when executed the Echo instruction is replaced by the instructions it replaced (e.g., see col. 1, lines 15-25 and col. 3,line 9-col. 4, line 31). With the instructions from the program stored in a memory one of ordinary skill would have been motivated to incorporate the Mohamed teachings of inserting a instruction means to prefetch the repetitive instructions from main memory to a instruction buffer prior to being executed to reduce the delay in accessing the repetitive instructions (e.g., see col.3, line 21-col. 4, line 39 of Mohamed).

6. Claims 1,20 contain the limitation the at least one index value referencing an area of an instruction storage unit. Mohamed taught this limitation (e.g., see col. 4, lines 23-60)[address pointer or index in address mapping table references an area of memory].

7. Claims 1,20 also include the limitation wherein the frequently executed instruction is accessible from the instruction storage unit using the at least one index value. Mohamed taught the explicit caching instruction stores a subset comprising a plurality of consecutive instructions from the set of instructions in association with an index value in plural storage elements (e.g., see col. 4, lines 22-60) each storage element associated with an index value, such that each one of the instructions can be retrieved with reference to the index value associated with the storage element (e.g. see col. 4, lines 22-60 and fig. 1).

8. As per claim 2, Fraser taught the step of identifying includes identifying a subset from the set of instructions comprising a plurality of instructions (e.g., see col. 3, lines 9-32).

9. As per claim 3, Fraser taught the subset comprises a plurality of consecutive instructions from the set of instructions (e.g., see col. 3, lines 9-32).

10. As per claim 4, Mohamed taught the explicit caching instruction directs an information processing device to store the subset of instructions stored in the storage unit in association with at least one index value (e.g., see col. col. 3, line 21-col. 4, line 60 and figs. 1,2).

11. As per claim 5, Mohamed taught the instruction storage element associated with the index value, such that the subset of instructions stored in the storage element can be retrieved with reference to the index value (e.g., see col. col. 3, line 21-col. 4, line 60 and figs. 1,2).

12. As per claim 6, Mohamed taught the instruction storage unit has a plurality of storage elements, each storage element associated with an index value and explicit caching instruction directed information processing device to store each instruction of the subset of instruction in one of the plurality of storage elements, such that each one of the instructions can be retrieved with reference to the index value associated with the storage element (e.g., see col. col. 3, line 21-col. 4, line 60 and figs. 1,2).

13. As per claim 7, Mohamed taught prefetching loops of instructions which would have been recognized by one of ordinary skill to applicable to outer loop subset and the subset of instructions part of an inner loop (e.g., see col. 3, lines 34-54 and col. 5, line

49-col, 6, line 24). One of ordinary skill would have been motivated to utilize the prefetching of the inner loops to take advantage of the reduced time for access to loop instructions when processing a nested loop of instructions.

14. As per claim 8, Mohamed taught the explicit caching instruction directs a node in an adaptive computing machine to store the identified instruction in an instruction storage unit in association with the index value (e.g., see col. col. 3, line 21-col. 4, line 60 and figs. 1,2).

15. As per claim 9, Mohamed taught the instruction storage unit has a storage element associated with the index value, such that the subset of instructions stored in the storage element can be retrieved with reference to the index value (e.g., see col. col. 3, line 21-col. 4, line 60 and figs. 1,2).

16. As per claim 10, Fraser taught the compressed instruction directs an information processing device to execute the identified instruction associated with the index value (e.g., see col. 10, lines 12-30).

17. Claims 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fraser (patent No. 6,907,598) in view of Mohamed (patent No. 6,684,319).

18. As per claim 13, Fraser taught (e.g. see fig. 7) when a program code is accessed and primary instruction retrieved is a Echo (or compressed) instruction within the instructions in memory retrieving from the instruction storage unit the at least one previously stored instruction unit using the compressed instruction and executing the previously stored instruction(s) (e.g., see col. 15, line16-col. 19, line 19). Fraser did not expressly detail the primary instruction being a explicit caching instruction. Mohamed

however taught for repetitive instruction blocks such as loops placing long instruction words in an instruction buffer where a prefetch flag bit is generated that facilitates copying the instructions from main memory to the prefetch instruction buffer. (e.g., see col. 2, lines 36-49). Mohamed taught that the prefetch instruction flag bit is sent from the compiler to the decoder. (e.g., see col. 3, lines 35-40) The Mohamed prefetch instruction flag bit is decoded several instructions before the prefetch instructions are decoded (e.g., see col. 3, lines 55-60). Since the use of the flag bit instructs the processor to perform an operation (namely prefetching of instruction(s) from main memory to cache) then it would have been obvious to one of ordinary skill the input to the decoder comprising the flag bit would have comprised an instruction. This is further evidenced since the decoder in the Mohamed system sends a signal to the prefetch instruction buffer control unit indicating the prefetch instruction flag bit was decoded and the prefetch instructions are to be written to a prefetch instruction buffer (e.g. col. 4 lines 1-7) and instructions are decoded from the compiler which are executed(e.g., see col. 3, lines 21-34).

19. It would have been obvious to one of ordinary skill to combine the teachings of Fraser and Mohamed. Both references were directed to the problems of processing repeated instructions in a DP system. (e.g., see 2, lines 35-45 of Mohamed and col. 2, lines 10-31). The Fraser system is further directed to problems with embedded system such as handheld computer systems, telephones etc. that have a relatively small amount of space. And the solution set forth in Fraser is to compress the instruction in the program replacing repetitive instruction with a Echo instruction ahead of time and

when executed the Echo instruction is replaced by the instructions it replaced (e.g., see col. 1, lines 15-25 and col. 3, line 9-col. 4, line 31). With the instructions from the program stored in a memory one of ordinary skill would have been motivated to incorporate the Mohamed teachings of inserting a instruction means to prefetch the repetitive instructions from main memory to a instruction buffer prior to being executed to reduce the delay in accessing the repetitive instructions (e.g., see col.3, line 21-col. 4, line 39 of Mohamed).

20. As per claims 14, 19 Mohamed taught the explicit caching instruction directs an information processing device to store the subset of instructions from the set of instruction (e.g., see col. 3,lines 21-60). Considering the Fraser teaching of compressing the instruction and retrieving the instruction for execution, the processing of compressed instruction would have retrieved and executed with an association with the index especially when the compressed instruction comprised instructions of a loop such was taught by Mohamed (e.g., see col. 4 lines 22-60 of Mohamed where an addressing table with starting and ending address pointers or indexes are used to access the prefetched instructions).

21. As per claim 15,16,17,18 Mohamed taught the explicit caching instruction stores a subset comprising a plurality of consecutive instructions from the set of instructions in association with an index value in plural storage elements (e.g., see col. 4, lines 22-60) each storage element associated with an index value, such that each one of the instructions can be retrieved with reference to the index value associated with the storage element (e.g. see col. 4, lines 22-60).

### *Allowable Subject Matter*

22. Claims 11-12, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

23. The change in scope of the amended claims has necessitated a new search.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-10,13-20 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER